AMENDMENTS TO CLAIMS

Please amend the claims as shown in the following listing of claims which will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended): A power amplifier comprising:

a plurality of amplification stages arranged on a die to permit an RF signal flow from one stage to the next stage with said RF signal flow being characteristic of a zig-zag pattern within at least a portion of said plurality of amplification stages; and

a DC bias circuitry centralized on said die, said circuitry providing a bias feed to each of said amplification stages;

wherein the plurality of amplification stages comprise a plurality of transistors ~~each having an input and an output,~~ and at least some of the transistors are arranged in a folded configuration; and

wherein ~~the~~ at least two of said plurality of amplification stages further comprise a compensation network coupled to a shared input of a transistor pair, signal splitter circuitry for providing substantially in-phase signals to the transistors; and combiner circuitry for in-phase combining outputs of the transistors.

2. (New): The power amplifier of claim 1, wherein said RF signal flows through at least two stages in said zig-zag pattern and then flows through said signal splitter circuitry and combiner circuitry.

3. (New): The power amplifier of claim 1, wherein said RF signal flows successively through said signal splitter circuitry, through at least two stages in said zig-zag pattern, and then through said combiner circuitry.

4. (New): A driver amplifier comprising a plurality of amplification stages, wherein at least two of said plurality of amplification stages are oriented such that an RF signal output of one of said plurality of amplification stages faces in the same direction as an

RF signal input of an adjacent amplification stage.

5. (New): The driver amplifier of claim 4, wherein each amplification stage comprises a plurality of transistors arranged in a folded configuration.

6. (New): A driver amplifier comprising:

a plurality of amplification stages arranged on a die to permit substantially all of an RF signal to flow from one stage to the next stage, and wherein said RF signal flow is characteristic of a zig-zag pattern; and

a DC bias circuitry centralized on said die, said circuitry providing a bias feed to each of said amplification stages.

7. (New): The driver amplifier of claim 6, wherein said amplification stages are arranged on said die such that the input of a first stage is orientated in the opposite direction of an adjacent stage.

8. (New): The driver amplifier of claim 7, wherein each amplification stage comprises a plurality of transistors, each having an input and an output, the transistors arranged in a folded configuration such that each of the transistors includes gate fingers with at least one of the transistors having gate fingers in vertical alignment with the gate fingers of another transistor.

9. (New): The driver amplifier of claim 7 further comprising a plurality of sections with each section having a plurality of FETs, said FETs arranged on a die in a folded FET configuration such that there is a shared gate connection of at least two of the FETs and a gate and a drain of at least two FETs are in vertical alignment, said sections arranged on a die in a folded amp configuration such that at least two of said sections represent mirrored images of each other.

10. (New): The driver amplifier of claim 7 configured in a folded amplifier configuration.

11. (New): A MMIC driver amplifier comprising:

a plurality of FET amplification stages with each stage having an RF signal input and an RF signal output, wherein at least two adjacent stages are orientated in opposite directions so that the output of one of said plurality of FET amplification stages is physically oriented in the opposite direction of the output of an adjacent one of said plurality of FET amplification stages;

a DC bias circuitry centralized on said die, said circuitry providing a bias feed to each of said amplification stages; and

an interstage matching network comprising said bias feed and a DC blocking capacitor.

12. (New): The MMIC driver amplifier of claim 11 configured to operate in one of the following band frequencies: K band, Ka band, and Ku band.

13. (New): A method of driver amplification, wherein the method comprises the steps of:

arranging a plurality of amplification stages on a die to permit substantially all of an RF signal to flow through said plurality of stages in a zig-zag manner;

supplying a DC bias to said plurality of amplification stages from a centralized DC bias circuitry on a perimeter of said die; and

wherein said plurality of amplification stages comprise at least two FET sections, wherein said at least two FET sections comprise a plurality of FETs and wherein said plurality of FETs are configured to have a shared input and shared output and are configured in a folded FET configuration.

14. (New): The method of claim 13 further comprising the step of forming at least two sections of FET's in a folded amplifier configuration.

15. (New): The method of driver amplification of claim 13, wherein said arranging step further comprises orientating adjacent stages in opposite directions.

16. (New): A driver amplifier comprising:

a plurality of amplification stages arranged on a die to permit an RF signal flow from one stage to the next stage, and wherein said signal flow is characteristic of a zig-zag pattern;

a DC bias circuitry centralized on said die, said circuitry providing a bias feed to each of said amplification stages; and

an interstage matching network comprising said DC bias feed and a DC blocking capacitor.

17. (New): A driver amplifier comprising a plurality of amplification stages, wherein each amplification stage comprises a transistor having an RF signal input and an RF signal output, the amplification stages physically oriented such that successive amplification stages are physically oriented 180 degrees from each other, such that the RF signal input is on a first side in a first amplification stage and on a second side in a second amplification stage, and wherein said second side is physically oriented in the opposite direction of said first side.

18. (New): A driver amplifier comprising a first transistor and a second transistor, wherein said first and second transistors each comprise a RF signal input and a RF signal output, wherein said RF signal input of said first transistor is oriented in a first direction, wherein said second transistor is physically adjacent to said first transistor, wherein said RF signal input of said second transistor is oriented in a second direction, and wherein said second direction is oriented 180 degrees from said first direction.

19. (New): A driver amplifier comprising:

a plurality of transistors;

a driver amplifier input on a first side of a chip, wherein said driver amplifier input is oriented in a first direction;

a driver amplifier output on a second side of said chip, wherein said driver amplifier output is oriented in a second direction, wherein each of said plurality of transistors comprises an RF signal input and an RF signal output, and wherein said RF signal input and RF signal output are oriented in directions that are substantially 90 degrees from said first and second directions.

20. (New): The driver amplifier of claim 19, wherein the orientation of said RF signal input and said RF signal output facilitates flow of a RF signal in a zig-zag path.